BRIDGE-TYPE MAGNETIC RANDOM ACCESS MEMORY (MRAM) LATCH

Abstract of the Disclosure

A technique to read a stored state in a magnetoresistive random access memory (MRAM) device, such as a giant magneto-resistance (GMR) MRAM device or a tunneling magneto-resistance (TMR) device uses a bit line in an MRAM device that is segmented into a first portion and a second portion. An interface circuit compares the resistance of a first portion and a second portion of a first bit line to the resistance of a first portion and a second portion of a second bit line to determine the logical state of a cell in the first bit line. The interface circuit includes a reset circuit that selectively couples the outputs of the interface circuit together. A subsequent decoupling of the outputs allows cross-coupling within the interface circuit to latch the outputs to a logical state corresponding to the stored magnetic state, thereby allowing the stored state of a cell to be read.

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